PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING SUBMISSION OR TRANSMITTAL OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

IWAHASHI, Fumio
Matsushita Electric Industrial
Co., Ltd.
1006, Oaza Kadoma
Kadoma-shi
Osaka 571-8501
JAPON

Date of mailing (day/month/year) 14 December 1999 (14.12.99)	
Applicant's or agent's file reference P21417-P0 松下寿 28920	**IMPORTANT NOTIFICATION**
International application No. PCT/JP99/05339 ✓	International filing date (day/month/year) 29 September 1999 (29.09.99) ✓
International publication date (day/month/year) Not yet published	Priority date (day/month/year) 30 September 1998 (30.09.98)
Applicant MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. et al	

1. The applicant is hereby notified of the date of receipt (except where the letters "NR" appear in the right-hand column) by the International Bureau of the priority document(s) relating to the earlier application(s) indicated below. Unless otherwise indicated by an asterisk appearing next to a date of receipt, or by the letters "NR", in the right-hand column, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).

2. This updates and replaces any previously issued notification concerning submission or transmittal of priority documents.

3. An **asterisk(*)** appearing next to a date of receipt, in the right-hand column, denotes a priority document submitted or transmitted to the International Bureau but not in compliance with Rule 17.1(a) or (b). In such a case, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

4. The **letters "NR"** appearing in the right-hand column denote a priority document which was not received by the International Bureau or which the applicant did not request the receiving Office to prepare and transmit to the International Bureau, as provided by Rule 17.1(a) or (b), respectively. In such a case, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

Priority date	Priority application No.	Country or regional Office or PCT receiving Office	Date of receipt of priority document
30 Sept 1998 (30.09.98)	10/277183	JP	22 Nove 1999 (22.11.99)

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DEC. 27. 1999
Center

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer

Taïeb Akremi TA

Telephone No. (41-22) 338.83.38

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF RECEIPT OF RECORD COPY

(PCT Rule 24.2(a))

To:

IWAHASHI, Fumio
Matsushita Electric Industrial
Co., Ltd.
1006, Oaza Kadoma
Kadoma-shi
Osaka 571-8501
JAPON

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Date of mailing (day/month/year)	IMPORTANT NOTIFICATION
20 October 1999 (20.10.99)	
Applicant's or agent's file reference 松下寿 28920 P21417-P0	**International application No.** PCT/JP99/05339 ✓

The applicant is hereby notified that the International Bureau has received the record copy of the international application as detailed below.

Name(s) of the applicant(s) and State(s) for which they are applicants:

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. (for all designated States except US)
NINOMIYA, Kunio et al (for US)

International filing date	:	29 September 1999 (29.09.99) ✓
Priority date(s) claimed	:	30 September 1998 (30.09.98)
Date of receipt of the record copy by the International Bureau	:	18 October 1999 (18.10.99)
List of designated Offices	:	

National :CN,ID,KR,SG,US

ATTENTION

The applicant should carefully check the data appearing in this Notification. In case of any discrepancy between these data and the indications in the international application, the applicant should immediately inform the International Bureau.

In addition, the applicant's attention is drawn to the information contained in the Annex, relating to:

- [X] time limits for entry into the national phase
- [X] confirmation of precautionary designations
- [X] requirements regarding priority documents

A copy of this Notification is being sent to the receiving Office and to the International Searching Authority.

RECEIVED DEC. 20. 1999 I.P.D.

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. (41-22) 740.14.35

Authorized officer:

Susumu Kubo

Telephone No. (41-22) 338.83.38

INFORMATION ON TIME LIMITS FOR ENTERING THE NATIONAL PHASE

The applicant is reminded that the "national phase" must be entered before each of the designated Offices indicated in the Notification of Receipt of Record Copy (Form PCT/IB/301) by paying national fees and furnishing translations, as prescribed by the applicable national laws.

The time limit for performing these procedural acts is **20 MONTHS** from the priority date or, for those designated States which the applicant elects in a demand for international preliminary examination or in a later election, **30 MONTHS** from the priority date, provided that the election is made before the expiration of 19 months from the priority date. Some designated (or elected) Offices have fixed time limits which expire even later than 20 or 30 months from the priority date. In other Offices an extension of time or grace period, in some cases upon payment of an additional fee, is available.

In addition to these procedural acts, the applicant may also have to comply with other special requirements applicable in certain Offices. **It is the applicant's responsibility** to ensure that the necessary steps to enter the national phase are taken in a timely fashion. Most designated Offices do not issue reminders to applicants in connection with the entry into the national phase.

For detailed information about the procedural acts to be performed to enter the national phase before each designated Office, the applicable time limits and possible extensions of time or grace periods, and any other requirements, see the relevant Chapters of Volume II of the PCT Applicant's Guide. Information about the requirements for filing a demand for international preliminary examination is set out in Chapter IX of Volume I of the PCT Applicant's Guide.

GR and ES became bound by PCT Chapter II on 7 September 1996 and 6 September 1997, respectively, and may, therefore, be elected in a demand or a later election filed on or after 7 September 1996 and 6 September 1997, respectively, regardless of the filing date of the international application. (See second paragraph above.)

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

CONFIRMATION OF PRECAUTIONARY DESIGNATIONS

This notification lists only specific designations made under Rule 4.9(a) in the request. It is important to check that these designations are correct. Errors in designations can be corrected where precautionary designations have been made under Rule 4.9(b). The applicant is hereby reminded that any precautionary designations may be confirmed according to Rule 4.9(c) before the expiration of 15 months from the priority date. If it is not confirmed, it will automatically be regarded as withdrawn by the applicant. There will be no reminder and no invitation. Confirmation of a designation consists of the filing of a notice specifying the designated State concerned (with an indication of the kind of protection or treatment desired) and the payment of the designation and confirmation fees. Confirmation must reach the receiving Office within the 15-month time limit.

REQUIREMENTS REGARDING PRIORITY DOCUMENTS

For applicants who have not yet complied with the requirements regarding priority documents, the following is recalled.

Where the priority of an earlier national, regional or international application is claimed, the applicant must submit a copy of the said earlier application, certified by the authority with which it was filed ("the priority document") to the receiving Office (which will transmit it to the International Bureau) or directly to the International Bureau, before the expiration of 16 months from the priority date, provided that any such priority document may still be submitted to the International Bureau before that date of international publication of the international application, in which case that document will be considered to have been received by the International Bureau on the last day of the 16-month time limit (Rule 17.1(a)).

Where the priority document is issued by the receiving Office, the applicant may, instead of submitting the priority document, request the receiving Office to prepare and transmit the priority document to the International Bureau. Such request must be made before the expiration of the 16-month time limit and may be subjected by the receiving Office to the payment of a fee (Rule 17.1(b)).

If the priority document concerned is not submitted to the International Bureau or if the request to the receiving Office to prepare and transmit the priority document has not been made (and the corresponding fee, if any, paid) within the applicable time limit indicated under the preceding paragraphs, any designated State may disregard the priority claim, provided that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity to furnish the priority document within a time limit which is reasonable under the circumstances.

Where several priorities are claimed, the priority date to be considered for the purposes of computing the 16-month time limit is the filing date of the earliest application whose priority is claimed.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

(PCT Rule 44.1)

To:
Matsushita Electric Industrial Co., Ltd.
Attn. Iwahashi, Fumio
1006, Oaza Kadoma, Kadoma-shi,
OSAKA 571-8501
JAPAN

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Date of mailing (day/month/year) 21/01/2000	
Applicant's or agent's file reference P21417-P0 松下寿 28920	FOR FURTHER ACTION See paragraphs 1 and 4 below
International application No. PCT/JP 99/05339 ✓	International filing date (day/month/year) 29/09/1999 ✓

Applicant

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. et al.

1. [X] The applicant is hereby notified that the International Search Report has been established and is transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the International Search Report; however, for more details, see the notes on the accompanying sheet.

Where? Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Facsimile No.: (41-22) 740.14.35

For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no International Search Report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

[ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

[ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Further action(s):** The applicant is reminded of the following:

Shortly after 18 months from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

Within 19 months from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within 20 months from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 19 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Liliane Van Velzen-Peron

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JAN. 26. 2000
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Form PCT/ISA/220 (July 1998)

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the PCT Applicant's Guide, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international pbulication. Furthermore, it should be emphasized that provisional protection is available in some States only.

What parts of the International application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Administrative Instructions, Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international appplication is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the same time of filing the amendments with the International Bureau, also file a copy of such amendments with the International Preliminary Examining Authority (see Rule 62.2(a), first sentence).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, where upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see Volume II of the PCT Applicant's Guide.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H04H 1/00, H04N 7/26

A1

(11) International Publication Number: **WO 00/19645**

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10/277183 30 September 1998 (30.09.98) JP

(71) Applicant *(for all designated States except US)*: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. [JP/JP]; 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 (JP).

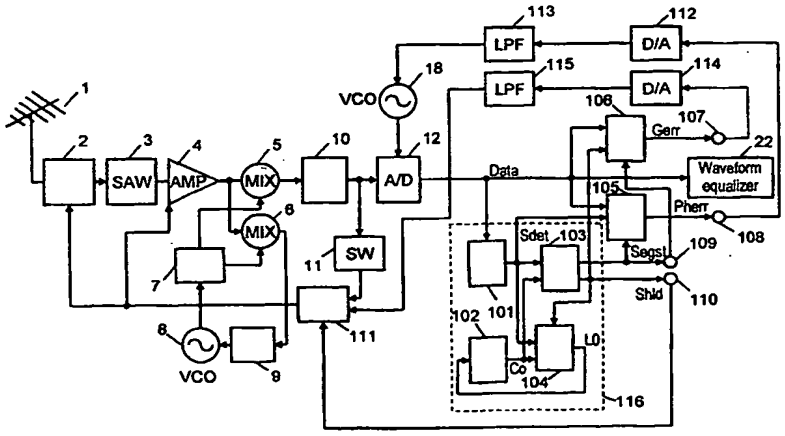
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: NINOMIYA, Kunio [JP/JP]; 1-9-151, Shonai-cho, Niihama-shi, Ehime 792-0811 (JP). SAKASHITA, Seiji [JP/JP]; 2-60-1-801, Minaminakaburi, Hirakata-shi, Osaka 573-0094 (JP). KATO, Hisaya [JP/JP]; 16-1-5, Hikaridai 8-chome, Seika-cho, Soraku-gun, Kyoto 619-0237 (JP).

(74) Agents: IWAHASHI, Fumio et al.; Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 (JP).

(81) Designated States: CN, ID, KR, SG, US.

Published
With international search report.

(54) Title: DEMODULATOR FOR DEMODULATING DIGITAL BROADCAST SIGNALS



(57) Abstract

A demodulator of digital terrestrial broadcast or the like for transmitting coded digital video and audio information in packet form comprises a synchronous code pattern detecting circuit for detecting the segment synchronous code pattern from the most significant bit signal of the reception packet data, a symbol number counter circuit for counting the number of symbol data in the reception packet data, a synchronism detection establishing circuit for judging the true segment synchronous code pattern by obtaining the segment synchronous code pattern from the synchronous code pattern detecting circuit when the symbol number counter circuit finishes counting of a specified number, and a synchronism detection protection counter circuit for detecting and establishing the segment synchronous signal in the reception data from the output of the synchronous code pattern detecting circuit and count-up of specified number of the symbol number counter circuit. In this constitution, even in an inferior environment for receiving broadcast such as deterioration of C/N of signal due to weak electric field, or strong ghost or multipath characteristic of terrestrial waves, the digital broadcast demodulator capable of processing packet synchronism detection, AGC, and clock regeneration stably and precisely is presented.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

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SPECIFICATION

DIGITAL BROADCAST DEMODULATOR

TECHNICAL FIELD

The present invention relates to a digital broadcast demodulator for demodulating a digital modulated signal modulated, for example, by multi-value VSB modulation, in digital broadcast for digital transmission by coding video and audio information.

BACKGROUND ART

Recently, owing to the advancement in the digital compression technology and digital modulation and demodulation technology, the television broadcast is presented by using satellites and CATV. The video data is coded by MPEG2, and the digital modulation system is realized by the QPSK method in satellite broadcast or QAM method in CATV. In the United States, the terrestrial digital broadcast (DTV) is scheduled from the fall of 1998, and the digital modulation 8VSB system by video compression by MPEG2 is planned.

Referring to the drawing, a conventional example of receiving and demodulating apparatus of digital terrestrial broadcast is explained below.

Fig. 10 is a block diagram of a demodulator of terrestrial digital broadcast. An RF modulated wave signal received by an antenna 1 which receives an RF signal is put into a tuner 2 which selects a channel, and an arbitrary channel is selected. In the tuner 2, the selected signal is controlled of gain, and converted in frequency, and is issued as an intermediate frequency (IF). The IF output from the tuner 2 is limited in band in the frequency characteristic determined in a SAW filter 3, and is put into an amplifier 4 which amplifies a signal.

In the amplifier4, by a control signal from an AGC detector 11

explained later, the signal level is controlled, and is supplied into mixers 5, 6. In the mixers 5, 6, the IF signal is multiplied by the local frequency signal from a voltage control oscillator 8 (VCO) to undergo quadrature detection. After quadrature detection, base band signals of I, Q signals are supplied into LPF 9 and LPF 10, individually.

Herein, the mixer 6 delivers a beat signal generated by the difference between the IF carrier frequency and the frequency signal from the VCO 8, and it is put into the LPF 9, and is supplied into the VCO 8 as frequency error signal. A reproduction carrier from the VCO 8 is put into the mixer 5, and a carrier delayed in phase by 90 degrees is supplied into the mixer 6 through a 90-degree phase shifter 7 for delaying the phase by 90 degrees. By constituting a PLL by the system of the mixer 6, LPF 9, VCO 8 and 90-degree phase shifter 7, the local signal equal to the IF carrier frequency of the reception modulated wave can be oscillated by the VCO 8.

The base band signal supplied into the LPF 10 is limited to a desired frequency characteristic, and is supplied into an A/D converter 12 for converting an analog signal into a digital signal, and the AGC detector 11 for determining the average of signal amplitude. In the AGC detector 11, detecting the envelope of the entered base band signal, an AGC control signal is generated. As the AGC control signal is fed back to the amplifier 4 and tuner 2 and controlled, the AGC operation is carried out.

On the other hand, the base band signal supplied into the A/D converter 12 is converted into a digital signal, and is supplied into a demodulation processing unit and a waveform equalizer 12 in a later stage. The digital data delivered from the A/D converter 12 is put into a BPF 13, and a half frequency component of the symbol frequency (Fs) of data speed is extracted.

Being supplied into a square circuit 14, the frequency component of Fs/2 is squared, and is put into a BPF 15. In the BPF 15, a frequency

component Fs equal to the symbol speed is extracted, and put into a phase detector 16 which detects a phase error. In the phase detector 16, a phase error from the symbol frequency (Fs) is detected, and supplied into a loop filter 17.

In the loop filter 17, the phase error signal is integrated, and supplied as control signal of VCO 18. By constituting the feedback loop to the BPF (Fs/2) 13, square circuit 14, BPF (Fs) 15, phase comparator 16, loop filter 17, and VCO 18, the clock is regenerated.

Further, the output digital data from the A/D converter 12 is supplied into a symbol judging circuit 19 for judging the value of the symbol data, and the value of the received symbol data is judged, and supplied into a synchronous signal detecting circuit 21 for detecting the synchronous signal in the reception data. In the synchronous signal detecting circuit 21, comparing with the symbol data value of the synchronous reference signal from a known data circuit 20 of synchronous signal for delivering the data value of known synchronous signal, the synchronous signal of packet data is detected.

Thus, in order to demodulate the digital terrestrial broadcast 8VSB or the like, important steps are synchronous signal detection processing of transmission packet data, AGC processing for controlling signal amplitude, and clock regeneration for extracting and regenerating clock component from transmission data.

However, in the event of occurrence of inferior environments for receiving broadcast, such as characteristic ghost and multipath of digital terrestrial broadcast, and same channel interference by NTSC or other analog broadcast, it is extremely difficult to detect the synchronism, operate the AGC or regenerated the clock precisely in such synchronous detection processing by precisely judging the data value of the symbol, AGC processing by determining the average of detected base band signals, or clock regeneration processing of extracting the frequency components in the transmission data. Accordingly, in order

to raise the precision, it was required to process by heightening the sampling frequency, or compose the filter by a considerably large circuit.

SUMMARY OF THE INVENTION

To solve the above problems, the digital broadcast demodulator of the invention is characterized by, in one aspect, comprising a circuit for establishing the synchronous signal in reception data by processing only the most significant bit (MSB) showing the positive or negative sign of the reception transport packet data.

In such constitution of the invention, even in an inferior radio wave condition of strong ghost or multipath interference characteristic of digital terrestrial broadcast, the synchronous signal in the packet can be detected and established stably by an extremely inexpensive circuit constitution.

It is a second aspect of the digital broadcast demodulator of the invention to regenerate the clock by phase control on the basis of a phase error, by determining the difference of synchronous signals of the reception packet data which should be originally at the same level, and detecting the clock phase error of transmission data.

In this constitution of the invention, by detecting the phase error of clock of reception data and feeding back to the VCO for controlling, even in an inferior radio wave condition of strong ghost, multipath interference or low C/N characteristic of digital terrestrial broadcast, the clock can be regenerated stably and precisely by an extremely inexpensive circuit constitution.

A third aspect of the digital broadcast demodulator of the invention is characterized by detecting the synchronous signal in the received packet data, determining the difference between the data value of the detected synchronous signal and the reference value, and controlling the AGC on the basis of this difference.

In this constitution of the invention, a precise AGC is realized even in an inferior radio wave condition.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a general block diagram of a digital broadcast demodulator of the invention, Fig. 2 is an essential block diagram of digital broadcast demodulator in a first embodiment of the invention, Fig. 3 is an essential block diagram of digital broadcast demodulator in a second embodiment of the invention, Fig. 4 is an essential block diagram of digital broadcast demodulator in a third embodiment of the invention, Fig. 5 is a data frame diagram of digital terrestrial broadcast VSB modulation system, Fig. 6 is a field synchronous signal diagram of digital terrestrial broadcast VSB modulation system, Fig. 7 is a sample waveform diagram of segment synchronous signal explaining the second embodiment of the invention, Fig. 8 is a waveform diagram of segment synchronous signal explaining the third embodiment of the invention, Fig. 9 is a block diagram of clock phase error detecting circuit of the invention, and Fig. 10 is a block diagram showing a constitution of a digital broadcast demodulator in a prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, preferred embodiments of the invention are described below. First in Fig. 1, the digital broadcast demodulator of the invention is described, particularly about the schematic constitution of the digital broadcast demodulator of digital terrestrial broadcast VSB modulation system, and then the embodiments corresponding to the claims of the invention are specifically described.

The parts having the same functions as in Fig. 10 showing a conventional reception demodulator of digital terrestrial broadcast are identified with same reference numerals, and detailed description is omitted.

Output digital data, Data, of an A/D converter 12 is divided into four portions. One of them is put into a synchronous (sync) code pattern detecting circuit 101 of a segment synchronism detection establishing circuit block 116, and synchronous pattern is detected by processing the code bit (most significant bit, MSB, showing positive or negative sign). The output of the synchronous code pattern detecting circuit 101 is divided into three portions, which are individually supplied into a detection protection counter circuit 103, a segment synchronism detection establishing circuit 104, and a clock phase error detecting circuit 105.

The output of the segment synchronism detection establishing circuit 104 for judging the true synchronous pattern of each segment is supplied into a symbol number counter 102 as a reset signal, and the counting result of the number of symbols in one packet is fed back into the detection protection counter 103 and segment synchronism detection establishing circuit 104. The detection protection counter 103 sends out a segment start signal Segst showing the position of the segment synchronous signal in the packet on the basis of the fed-back information to a terminal 109, and a segment synchronism establishment signal Shld showing the detection establishment of the segment synchronous signal to a terminal 110.

The segment synchronism establishment signal Shld is put into a switch circuit 111 to become a switch signal for changing over a control signal Gerr from an AGC error detecting circuit 106 mentioned below and a control signal from the AGC detector circuit 11.

The second output digital data, Data, branched from the A/D converter 12 is supplied into the clock phase error detecting circuit 105, and is fed together with the signal from the synchronous code pattern detecting circuit 101 and the segment start signal Segst from the detection protection counter 103, and a clock phase error of data is issued as clock regeneration control signal Pherr to the terminal 108.

This clock regeneration control signal Pherr is put into a D/A converter 112, and is converted into an analog signal, which is fed into the LPF 113. The control signal integrated in the LPF 113 is put into the VCO 18 to control its oscillation frequency. A feedback loop is composed in the flow of the VCO 18, A/D converter 12, clock phase error detecting circuit 105, D/A converter 112, and LPF 113.

Further, the third divided output of digital data, Data, of the A/D converter 12 is put also into the AGC error detecting circuit 106, and issued into the terminal 107 as an AGC control signal Gerr as the different from the known value. This AGC control signal Gerr is put into the D/A converter 114, and is converted into an analog signal, and is supplied into the LPF 115. The AGC control signal integrated in the LPF 115 is supplied into the switch circuit 111.

The switch circuit 111 changes over, by the segment establishment signal Shld, between the control signal from the analog AGC detector 11 and the AGC control signal from the LPF 115 detected by digital processing. The AGC control signal as output from the switch circuit 111 is put into the amplifier 4 and tuner 2, and the amplitude of the input signal is controlled.

The fourth output of the A/D converter 12 is put into the waveform equalizer 22 to be a reception output.

In thus constituted digital broadcast demodulator, specific embodiments corresponding to the claims are described below.

(Embodiment 1)

Fig. 2 shows an essential block diagram of the embodiment corresponding to claims 1, 2, 3 of the invention. This embodiment relates to a digital broadcast demodulator used in an apparatus for receiving digital broadcast by transmitting coded digital video and digital audio information in packet form, in which, particularly in digital VSB transmission system, the circuit is constituted to process the code bit (MSB) of reception transport packet data, and the

synchronous signal in the reception data is established. In this constitution, even in an inferior radio wave condition for receiving broadcast, such as ghost, multipath, or same channel interference of NTSC, the synchronous signal in the packet can be detected and established precisely and securely.

Referring now to Fig. 2, the constitution and operation are described below. In the demodulator of the invention, the base band signal after quadrature detection is put into the A/D converter 12, and the clock regeneration has been already locked. Of the output digital data, Data, from the A/D converter 12, the code bit (MSB) is supplied into the synchronous code pattern detecting circuit 101 and symbol number counter 102 in the segment synchronism detection establishing circuit block 116. Herein, the data structure of packet of VSB digital terrestrial broadcast is shown in Fig. 5 and Fig. 6. The transmission frame shown in Fig. 5 is composed of 832 symbols in one packet, and the segment synchronous signal is inserted by the portion of four symbols only from the beginning.

In every 313 packets (segment), field synchronous signals #1, #2 are inserted. Fig. 6 shows the field synchronous signal. At the beginning of the packet, a segment synchronous signal of four symbols, and a specific number of PN codes are composed. The segment synchronous signal is a mapping signal in the values of +5, -5, -5, +5 as shown in Fig. 6. This signal value is the known data, and is inserted at the beginning of all packets as shown in Fig. 5.

In the synchronous code pattern detecting circuit 101, the code bit (MSB) of all reception data is processed, and +, -, -, + as code pattern of segment synchronous signal are detected. When processing the signal by the complement of 2, the codes of the segment synchronous signal are -, +, +, -.

When processing the code bits only, even in the presence of strong ghost, multipath interference or NTSC same channel interference

characteristic of digital terrestrial broadcast, the reception data receives considerably effects of impedance, and deterioration occurs. However, the code bit information is extremely strong against effects of interference even in the inferior reception wave situation, so that the synchronous pattern of the segment synchronous signal can be detected stably.

When detecting the synchronous pattern for four symbols in all reception data in the synchronous code pattern detecting circuit 101, simultaneously, signal Sdet is issued to the detection protection counter 103 and segment synchronous detection establishing circuit 104. In the symbol number counter 102, when the power is supplied, power-on reset is applied and synchronized with the signal processing clock equal to the symbol speed Fs, thereby starting automatic count-up. When counting 832 symbols in one packet, a count-up signal Co is issued to the detection protection counter 103 and segment synchronism detection establishing circuit 104.

In the segment synchronism detection establishing circuit 104, synchronous pattern detection signal Sdet, symbol number count-up signal Co, and signal Shld from detection protection counter 103 are supplied, if there is same pattern as the segment synchronous code pattern in all reception data, it is judged which pattern is the true segment synchronous signal.

In the operation of the segment synchronism detection establishing circuit 104, when either the signal Co issued when the symbol number counter 102 reaches the symbol number count 832 of the packet, or the segment synchronous code pattern detection signal Sdet from the synchronous code pattern detecting circuit 101 is entered, an output signal Lo is issued.

Usually, in the reception data, there are many code pattern data same as the segment synchronous code pattern, but the symbol number counter 102 is once reset when the same code pattern detection signal

Sdet as the segment synchronous signal is fed into the segment synchronism detection establishing circuit 104, and Lo signal for dropping to Low by the portion of one clock is entered, and counts up to 832 which is the number of symbols in one packet. In the midst of counting up, when the same pattern as the synchronous code pattern is detected, the segment synchronism detection establishing circuit 104 issues signal Lo and resets the symbol number counter 102. Thus, the counting operation is repeated until the signal Sdet is entered simultaneously with the output of signal Co of count-up of symbol number 832 of one packet. That is, in the case of a true segment synchronous signal, when counting of 832 is over, simultaneously, there is a segment synchronous signal of next packet, and the signal Sdet and signal Co are simultaneously entered into the segment synchronism detection establishing circuit 104, and Lo signal is issued, and the symbol number counter 102 is reset.

The output signal Co of the symbol number counter 102 and the output signal Sdet of the synchronous pattern detecting circuit 101 are also supplied into the detection protection counter 103. As a result, the detection protection counter 103 sets high the hold signal Shld once every time, and by this signal Shld, the segment synchronism detection establishing circuit 104 is held, and it is held in the state that the reset signal Lo is not issued until the signal Sdet from the circuit 101 and signal Co from the circuit 102 are entered simultaneously. Therefore, if only Sdet signal is entered in the meantime, the reset signal Lo is not issued. At this first time, however, if signal Co is next entered in the circuit 103, unless the signal Sdet is entered at the same time, the symbol number counter 102 and detection protection counter 103 are reset, and the signal Shld is low. In the detection protection counter 103, counting the number of times of simultaneously input of signal Sdet and signal Co, and when Sdet and Co are entered simultaneously by the specified number of times, for example, four times

consecutively, it is detected and established as the true segment synchronous signal in the reception data. The reason is that, in the case of output of signal Co, it is possible that signal of same pattern, but not the true segment synchronous signal may entered by accident, and such possibility is avoided. Thus, when the segment synchronous signal in the reception data is detected and established repeatedly by a specified number of times, the segment establishment signal Shld is fixed at high level.

By this Shld signal, the segment synchronism detection establishing circuit 104 is held, and it is held in the state that the reset signal Lo is not issued until the Sdet signal from the circuit 101 and Co signal from the circuit 102 are entered at the same time. Therefore, if only Sdet signal is entered in the meantime, the reset signal Lo is not issued. Even in this hold state, only when the signal Sdet and signal Co are entered simultaneously, reset signal Lo is issued, and the symbol number counter 102 is updated.

Once the segment synchronous signal is established, if signal Sdet and signal Co are not entered simultaneously, the segment establishment is not canceled immediately, but when making mistakes by a specified number of times, for example, eight times or more, the establishment of segment synchronous signal detection is canceled, and the signal Shld is set to low level.

Thus, while resetting the symbol number counter 102 every time the same waveform as the segment synchronous signal is detected, when reset by a true segment synchronous signal and similar waveform to the synchronous signal is not entered until counting up the specified number, count-up of the symbol number counter 102 and incoming of true synchronous signal of next segment occur simultaneously, and signal Shld is issued from the detection protection counter, and similar waveform while counting up the circuit 102 is eliminated, and when this operation is repeated by a specified number of times, it is detected and established

as true segment synchronous signal.

The constitution of this embodiment comprises the synchronous code pattern detecting circuit 101 for detecting the known synchronous signal code pattern by processing only the code bit (MSB) of the reception data, symbol number counter 102 for counting the number of symbols in one packet, segment synchronism detection establishing circuit 104 for judging true segment synchronous code pattern when the symbol number counter 102 detects the specified count while detecting the synchronous signal code pattern at the same time, and issuing a signal for resetting the symbol number counter 102, and detection protection counter circuit 103 for issuing signal Shld by detecting and establishing the segment synchronous signal in the reception data from the output of the synchronous code pattern detecting circuit 101 and the count-up of specified number of the symbol number counter circuit 102, and therefore even in an inferior radio wave condition for receiving broadcast such as strong ghost or multipath characteristic of digital broadcast, same channel interference of NTSC broadcast, low C/N, and others, the synchronous signal can be detected and established stably, and decoding can be processed stably.

(Embodiment 2)

Fig. 3 shows a block diagram of embodiment 2 corresponding to claims 4, 5, 6, 7 of the invention. This embodiment relates to a digital broadcast demodulator used in an apparatus for receiving digital broadcast by transmitting coded digital video and audio information in packet form, in which, particularly in digital VSB transmission system, the clock phase error of reception data is obtained by calculating the difference of N-th and N+1-th (N > 1) packet synchronous signals of reception data, and the clock is regenerated stably even in an inferior radio wave reception circumstance.

Referring now to Fig. 3, the constitution and operation are described below. The broken line block 116 corresponds to the segment

synchronism detection establishing circuit block shown in Fig. 2 of embodiment 1, and it issues the segment synchronism establishing signal Shld showing establishment of detection of segment synchronous signal in the reception data, Data, and segment start signal Segst showing the position of the segment synchronous signal in the packet. The operation of block 116 is same as explained in embodiment 1, and is omitted.

The reception digital data output, Data, from an A/D converter 12 is put into a clock phase error detecting circuit 105. The segment synchronism detection establishing circuit block 116 also feeds the signal Sdet showing the position of the same data as the code pattern of the synchronous signal in the packet data and the signal Segst showing the position of segment signal in the packet data.

Fig. 9 shows a block diagram of clock phase error detecting circuit 105. The digital data, Data, from the A/D converter 12 is put into an addition input of an subtracting circuit 202 through a latch 203. This input is further put into a subtraction input of the subtracting circuit 202 through a latch 204. In the subtracting circuit 202, the N-th input is subtracted from the N+1-th input, and the subtraction value is put into a latch circuit 207. The sequence of subtraction operations is not limited, but it is important whether the value becomes 0 or not. In the latch circuit 207, the data is latched by the signal Sdet of code pattern detection of segment synchronous signal, and issued into a latch circuit 208. The signal Sdet is adjusted in time so as to latch the subtraction value at the timing after subtraction operation of the second and third segment synchronous signals of reception data by the latch circuit 205. In the latch circuit 208, by latching by the signal Segst showing the position of the segment synchronous signal to be sent out after detecting and establishing the segment synchronous signal, it is sent out as clock phase error signal Pherr. The signal Segst is also adjusted in time to the timing to be latched by the latch circuit 208, by the subtracted values of the second and third segment synchronous

signals in the latch circuit 206.

This circuit is constituted so as to detect segment synchronous signals of four symbols as shown in Fig. 7, and if using a different code pattern, the circuit may be composed differently.

Fig. 7 shows sample points of thus obtained segment synchronous signal unit. The sample points are a, b, c, d when the oscillation frequency of the VCO 18 is completely matched in phase with the clock of the reception data. The data values are smooth values because the band is limited so as not to cause inter-code interference by filtering processing of the SAW filter 3 in the preceding stage. Herein, supposing the N-th data to be the second data value b, by subtraction from the N+1-th data value c, c-b is processed.

As shown in Fig. 7, the subtraction processing is to determine the inclination of the linking line of sample point values b and c, or b' and c', which should be originally of the same level. Herein, when the clock of the reception data and the phase of the frequency signal oscillated by the VCO 18 are synchronized completely, the value of c-b is 0. If the frequency or phase is deviated, as indicated by broken line in Fig. 7, it is like c'-b', and the clock phase error signal Pherr is determined by subtraction process. Feedback control is executed so that this clock phase error signal Pherr may be close to 0. As shown in Fig. 1, the clock phase error is fed into the D/A converter 112 to be converted into an analog signal, and is supplied into the LPF 113. The clock phase error converted into analog signal is integrated in the LPF 113, and is supplied into the VCO 18 as clock phase control signal. In the VCO 18, the oscillation frequency signal is controlled on the basis of the clock phase control signal, and it is synchronized with the clock signal of the reception data by the PLL. In this example, the level is compared between two consecutive signals which should be originally of the same level, but if not consecutive, the level may be compared between two signals which are supposed to be of the same level

by nature.

Incidentally, according the invention as set forth in claim 7, when turning on the power or changing over the channels, until the segment synchronous signal of the packet is detected and established, it is intended to finish the clock regeneration quickly by feeding back the differential value of all data that should be originally of the same level matched between the synchronous signal and code pattern in the packet data, continuously to the VCO 18 as clock phase error.

In this embodiment, from the signal Segst showing the position of the synchronous signal of the data being sent out in packet form and the signal Sdet showing the synchronous signal in the packet data and the code pattern are the same data, the N-th and N+1-th synchronous signals of the packet data which are originally of the same level are processed by subtraction, and the clock phase error signal Pherr is determined, and the clock regeneration process is executed to control so that the error may be 0.

In this constitution, even in an inferior radio wave condition for receiving digital broadcast, the clock regeneration is realized stably in a very simple and inexpensive circuit constitution.

(Embodiment 3)

Fig. 4 shows a block diagram of embodiment 3 corresponding to claims 8, 9, 10 of the invention. This embodiment presents a digital broadcast demodulator, that is, a digital broadcast demodulator for receiving digital broadcast by transmitting coded digital video and audio information in packet form, in which, particularly in digital VSB transmission system, the synchronous signal is detected in the received packet data, and from the synchronism detection establishment signal and the signal showing the position of the synchronous signal in the packet, the difference between the data value of synchronous signal and the reference value is calculated, and thereby AGC is realized.

Referring now to Fig. 4, the constitution and operation are

described below. The broken line block 116 corresponds to the segment synchronism detection establishing circuit block shown in embodiment 1, and it issues the segment synchronism establishing signal Shld showing establishment of detection of segment synchronous signal in the reception data, Data, and segment start signal Segst showing the position of the segment synchronous signal in the packet. The operation of block 116 is same as explained in embodiment 1, and is omitted. The digital data output, Data, from an A/D converter 12 is put into an AGC error detecting circuit 106.

Fig. 8 shows segment synchronous signals of four symbols added to the beginning of packet data. The segment synchronous signal is mapped in the values of ± 5 as shown in Fig. 8. Since these are known values, at the reception side, the data values corresponding to ± 5 may be possessed as reference values. When the segment synchronism establishing signal Shld is entered in the AGC error detecting circuit 106, from the signal Segst showing the position of the segment synchronous signal in the packet, the position of the data of four symbols from the beginning of the segment synchronism is specified, and the difference of this value and the internal reference value is determined. As shown in Fig. 8, when the reception data is entered as indicated by broken line, the difference from the reference value is as indicated by d at the + side, and d' at the - side. Feedback control is executed so that the differences d, d' from the reference value may be closer to 0.

This is to show a case in which reception data larger than the reference value of segment synchronous signal is entered, but when data smaller than the reference value is entered, by subtracting after absolute value processing so that the code may not be inverted by subtraction process to increase the differential value, the error signal Gerr is issued as AGC control signal. The AGC control signal Gerr is put into the D/A converter 114 from the terminal 107 as shown in Fig.

1', and is converted into an analog signal and is supplied into the LPF 115. The AGC control signal integrated by the LPF 115 is fed into the amplifier 4 and tuner 2 through the switch circuit 111, and by feedback control, the amplitude of the reception data is controlled to realize AGC.

According to claim 10 of the invention, when turning on the power or changing over the channels, until the segment synchronous signal in the packet data is detected and established, it is intended to change over the AGC control signal between the control signal of detecting the amplitude error from the envelope of the analog signal and the control signal of detecting the amplitude error from the synchronous level by digital processing, by supplying the segment synchronism establishing signal Shld issued from the terminal 110 shown in Fig. 1 into the switch circuit 111. When the reception data is entered, until the segment synchronous signal of the packet is detected and established, the amplitude error is detected from the envelope of the base band signal by analog detection in the analog processing unit in the preceding stage, and the AGC control on the basis of this error is applied by priority, and after detecting and establishing the segment synchronous signal in the packet, the error signal from digital processing for detecting the amplitude error from the synchronous signal is fed back, and the AGC is done efficiently.

In this embodiment 3, from the signal Segst showing the position of synchronous signal of data sent in packet form, and the signal Shld showing the detection and establishment of the synchronous signal, by subtraction processing of the segment synchronous signal of reception data and reference value of segment signal, the amplitude error signal Gerr is determined, and D/A converted, and integrated by LPF, and fed back to the analog amplifier and tuner through the switch circuit 111, there by controlling the amplitude and realizing AGC. In this method, even in an inferior radio wave condition for receiving digital broadcast,

such as ghost and multipath, the AGC is realized stably in a very inexpensive circuit constitution.

In the foregoing embodiments, the demodulator of terrestrial digital broadcast is shown, but it may be also applied in other applications.

The number of symbols, the number of segments, the constitution of pulses of parts, and detail of signal format may be changed or modified within the scope of the claims.

Of course, the operation of individual circuits in the embodiments may be also realized by processing of microprocessor.

INDUSTRIAL APPLICABILITY

As described herein, the digital broadcast demodulator of the invention, relating to digital terrestrial broadcast of packet data or the like, comprises a synchronous pattern detecting circuit for processing code bits of reception data and detecting synchronous signal pattern, a symbol number counter circuit, a synchronism detection protection counter circuit, and a synchronism detection establishing circuit, in which the true synchronous signal pattern is established and detected, and therefore even in an inferior radio wave condition, such as strong ghost and multipath interference characteristic of digital terrestrial broadcast, the synchronous signal in the packet can be established and detected stably in a very inexpensive circuit constitution.

Also comprising subtracting means of reception data, by determining the level difference between synchronous signals which should be of the same level by nature, from the same code pattern detection signal as the synchronous signal and the signal showing the position of synchronous signal in the packet, the clock phase error of reception data is detected, and fed back to the VCO for controlling, and therefore even in an inferior radio wave condition, such as strong ghost and

multipath interference characteristic of digital terrestrial broadcast, low C/N, and others, the clock can be regenerated stably and precisely in a very inexpensive circuit constitution.

Further, by subtracting the synchronous signal of reception data and known reference value from the signal showing the position of synchronous signal in the reception packet data and the signal detecting and establishing the synchronous signal in the packet data, the amplitude error is determined, and fed back to the analog amplifier circuit and tuner for controlling, so that precise AGC is realized even in an inferior radio wave environment.

CLAIMS

1. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form, comprising:

a circuit for establishing the synchronous signal in reception data by processing the most significant bit (MSB) showing the positive or negative sign of the reception transport packet data.

2. A digital broadcast demodulator of claim 1, wherein the circuit for establishing the synchronous signal in reception data comprises:

a synchronous code pattern detecting circuit for detecting the segment synchronous code pattern from the most significant bit signal of the reception packet data,

a symbol number counter circuit for counting the number of symbol data in the reception packet data,

a synchronism detection establishing circuit for judging the true segment synchronous code pattern by obtaining the segment synchronous code pattern from said synchronous code pattern detecting circuit when said symbol number counter circuit finishes counting of a specified number, and

a synchronism detection protection counter circuit for detecting and establishing the segment synchronous signal in the reception data from the output of said synchronous code pattern detecting circuit and count-up of specified number of said symbol number counter circuit.

3. A digital broadcast demodulator of claim 2, wherein the most significant bit signal of the reception packet data is processed so as to issue a signal showing the start position of the synchronous signal in the data and a signal of detecting and establishing the synchronous signal.

4. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein the differential value of synchronous signals of reception packet data which should be of same level by nature is determined so as to detect the clock phase error of transmission data, and the clock is regenerated by phase control on the basis of this phase error.

5. A digital broadcast demodulator of claim 4, further comprising a clock phase error detecting circuit for issuing a clock phase error of transmission data by determining the difference of the N-th and N+1-th (N>1) synchronous signals which should be of same level by nature, from the code pattern detection signal of synchronous signal and signal showing position of synchronous signal.

6. A digital broadcast demodulator of claim 4, further comprising:

a circuit for processing the difference of all reception data,

a circuit for detecting the differential value only for the data coinciding with the code pattern of synchronous signal, and

a circuit for detecting the differential value only for the data of synchronous signal.

7. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein the clock is regenerated by detecting the clock phase error from the differential value of the data which should be of same level by nature coinciding with the synchronous signal code pattern of reception data until the synchronous signal of reception packet data is detected and established.

8. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio

information coded by digital VSB modulation system in packet form,

wherein the synchronous signal in the received packet data is detected, the difference between the detected data value of synchronous signal and the reference is determined, and the AGC is realized on the basis of this difference.

9. A digital broadcast demodulator of claim 8, further comprising an AGC error detecting circuit for detecting a specific position of synchronous signal from the signal showing detection and establishment of synchronous signal in the reception data and the signal showing position of synchronous signal, and issuing the error of the synchronous signal at this specific position and the reference value as a control signal.

10. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein the AGC is realized by detecting the amplitude difference from the envelope of analog detected base band signal until the synchronous signal of reception packet data is detected and established.

ABSTRACT

A demodulator of digital terrestrial broadcast or the like for transmitting coded digital video and audio information in packet form comprises a synchronous code pattern detecting circuit for detecting the segment synchronous code pattern from the most significant bit signal of the reception packet data, a symbol number counter circuit for counting the number of symbol data in the reception packet data, a synchronism detection establishing circuit for judging the true segment synchronous code pattern by obtaining the segment synchronous code pattern from the synchronous code pattern detecting circuit when the symbol number counter circuit finishes counting of a specified number, and a synchronism detection protection counter circuit for detecting and establishing the segment synchronous signal in the reception data from the output of the synchronous code pattern detecting circuit and count-up of specified number of the symbol number counter circuit.

In this constitution, even in an inferior environment for receiving broadcast such as deterioration of C/N of signal due to weak electric field, or strong ghost or multipath characteristic of terrestrial waves, the digital broadcast demodulator capable of processing packet synchronism detection, AGC, and clock regeneration stably and precisely is presented.

FIG. 1

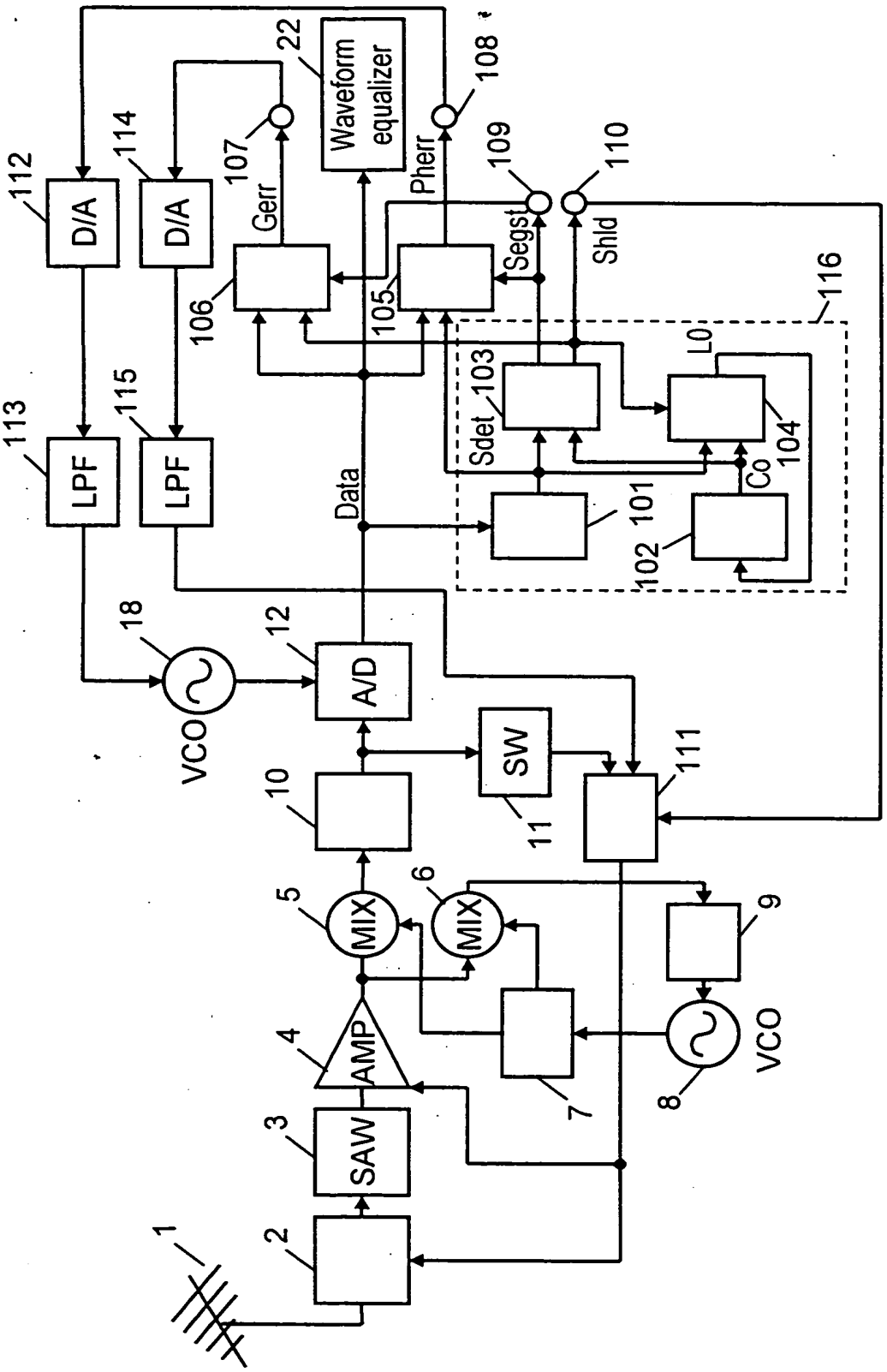

1
2
3
SAW
4
AMP
5
MIX
6
MIX
7
8
VCO
9
10
11
SW
111
12
A/D
18
VCO
112
D/A
114
D/A
113
LPF
115
LPF
107
Gerr
22
Waveform equalizer
108
Pherr
109
Segst
110
Shld
106
105
116
Sdet
103
LO
104
Co
Data
101
102

FIG.2

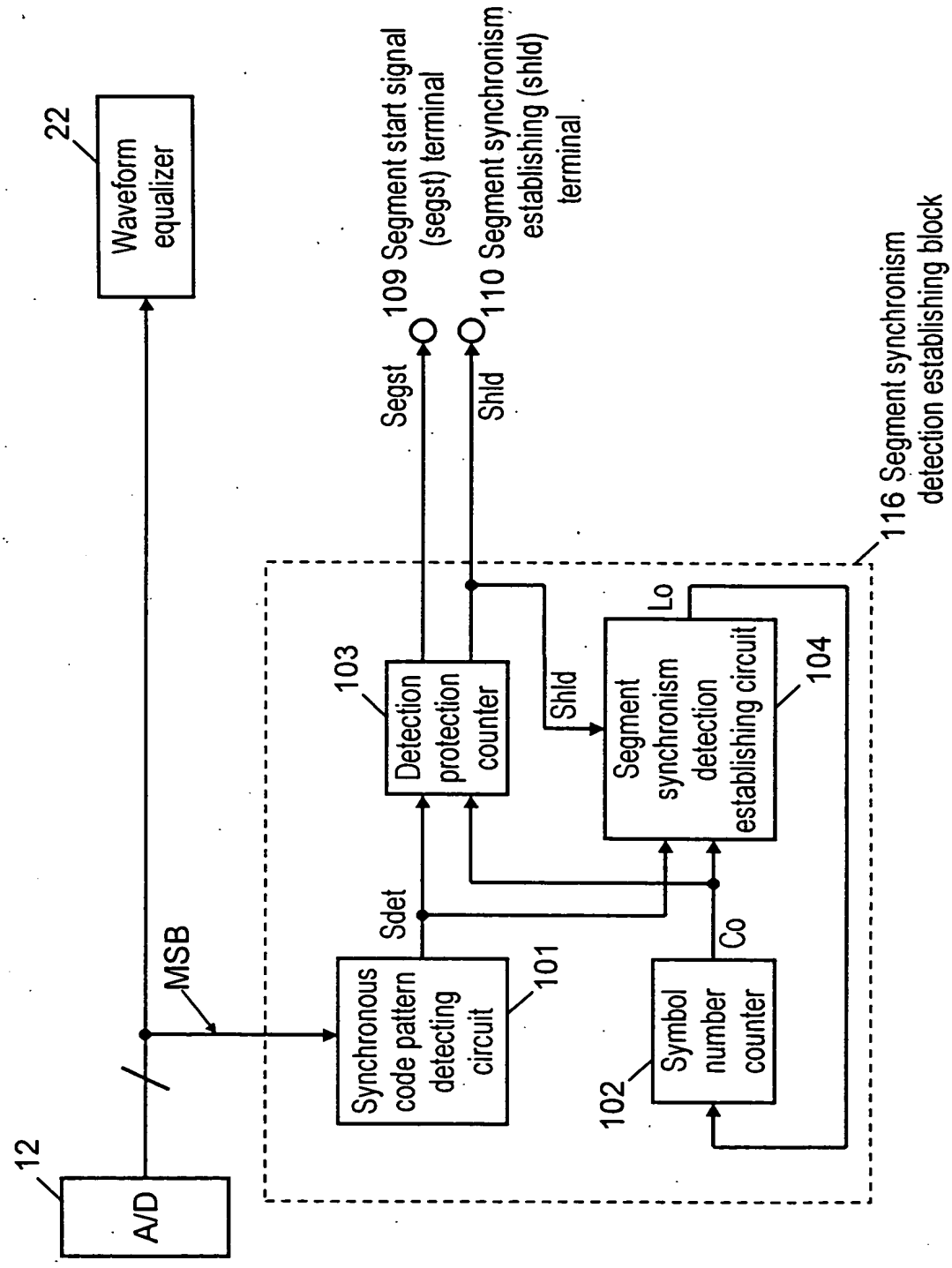

22
Waveform equalizer
109 Segment start signal (segst) terminal
110 Segment synchronism establishing (shld) terminal
Segst
Shld
116 Segment synchronism detection establishing block
Lo
103
Detection protection counter
Shld
Segment synchronism detection establishing circuit
104
Sdet
Co
MSB
Synchronous code pattern detecting circuit
101
Symbol number counter
102
12
A/D

FIG. 3

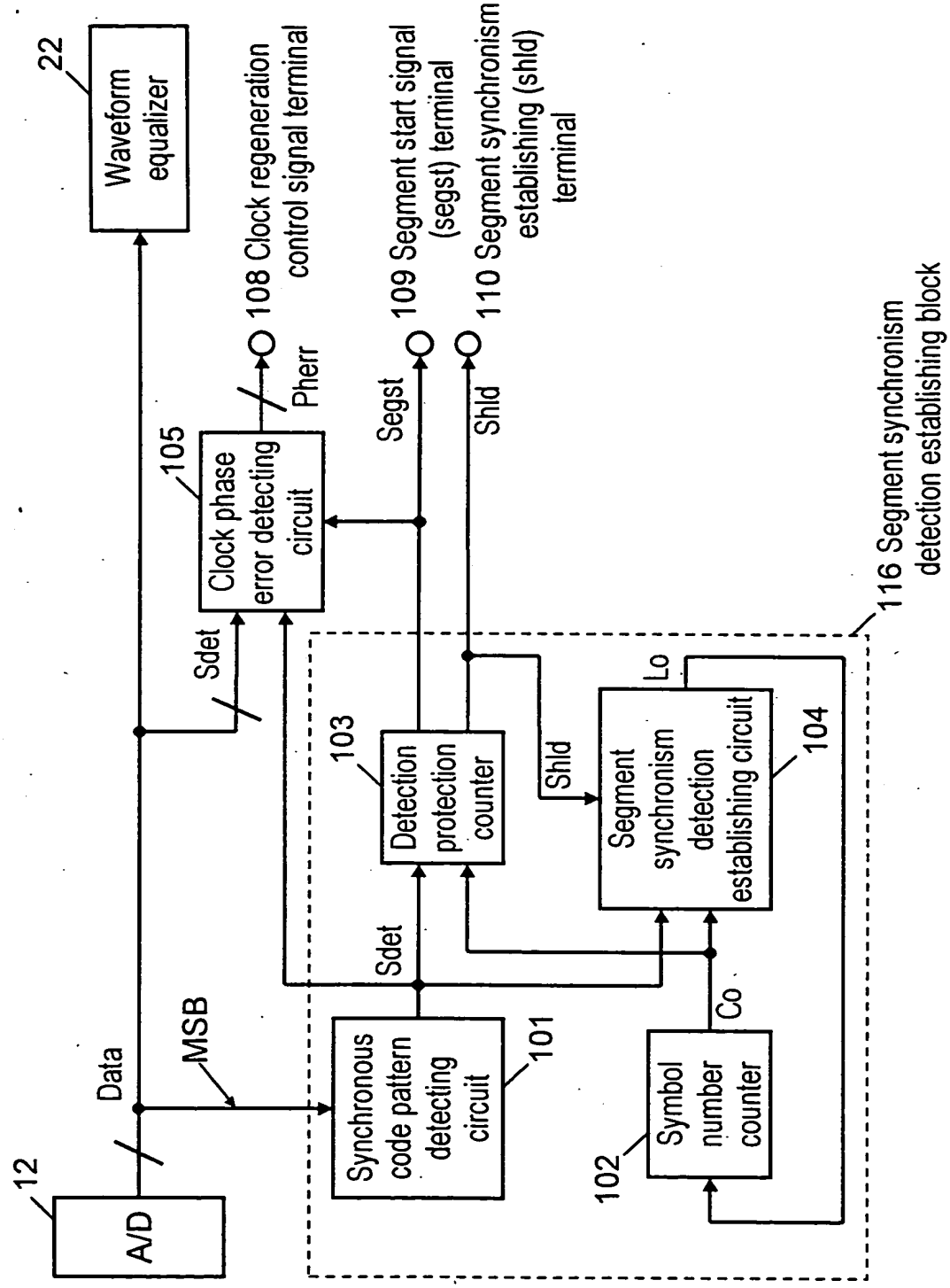

22
Waveform equalizer
108 Clock regeneration control signal terminal
109 Segment start signal (segst) terminal
110 Segment synchronism establishing (shld) terminal
Pherr
Segst
Shld
105
Clock phase error detecting circuit
Sdet
116 Segment synchronism detection establishing block
103
Detection protection counter
Shld
Lo
Segment synchronism detection establishing circuit
104
Sdet
Data
MSB
Synchronous code pattern detecting circuit
101
Co
12
A/D
102
Symbol number counter

FIG. 4

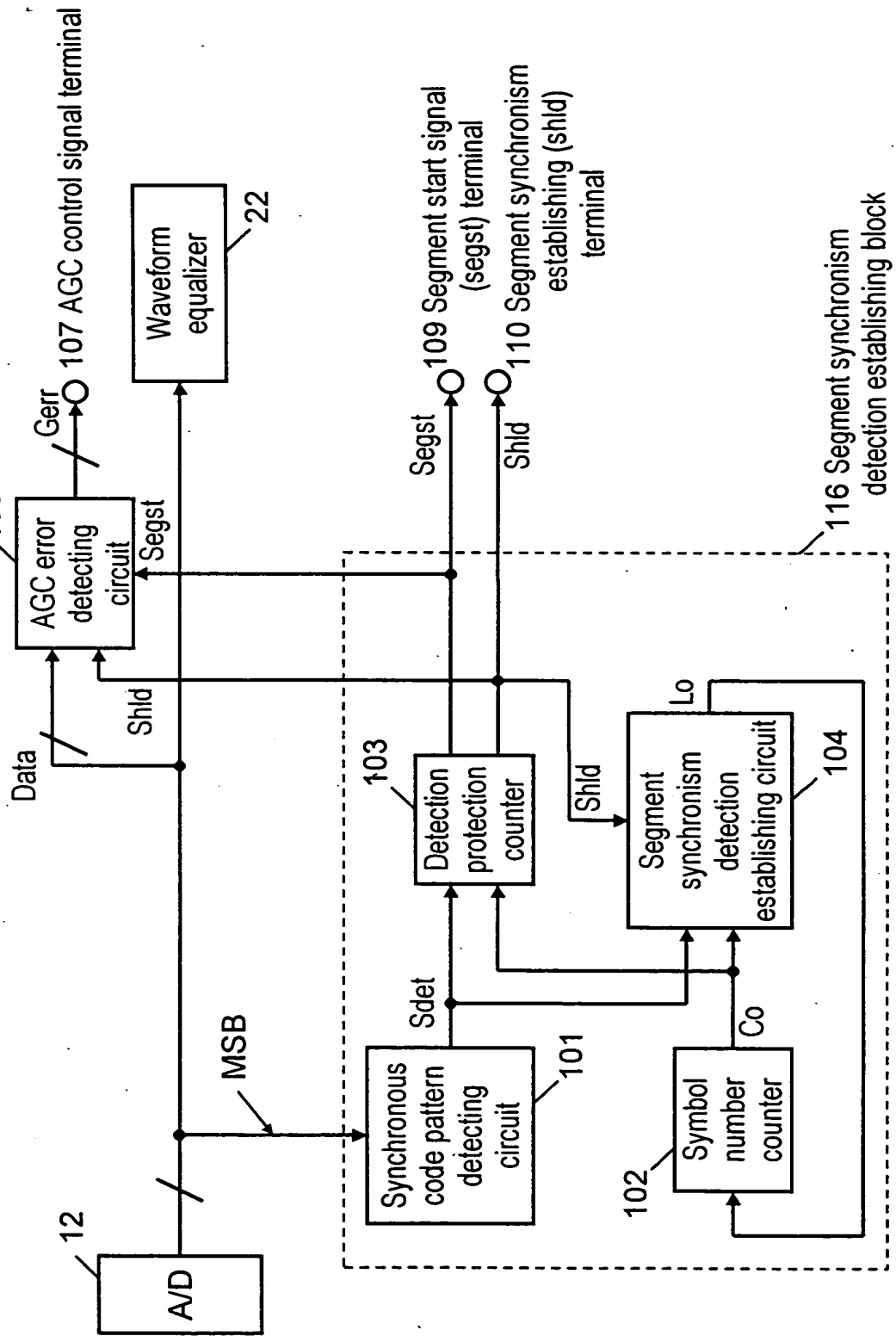

12
A/D
MSB
Synchronous code pattern detecting circuit
101
Sdet
Detection protection counter
103
Segst
109 Segment start signal (segst) terminal
Shld
110 Segment synchronism establishing (shld) terminal
Segment synchronism detection establishing circuit
104
Lo
Co
Symbol number counter
102
116 Segment synchronism detection establishing block
Waveform equalizer
22
107 AGC control signal terminal
Gerr
AGC error detecting circuit
106
Segst
Shld
Data

FIG. 5

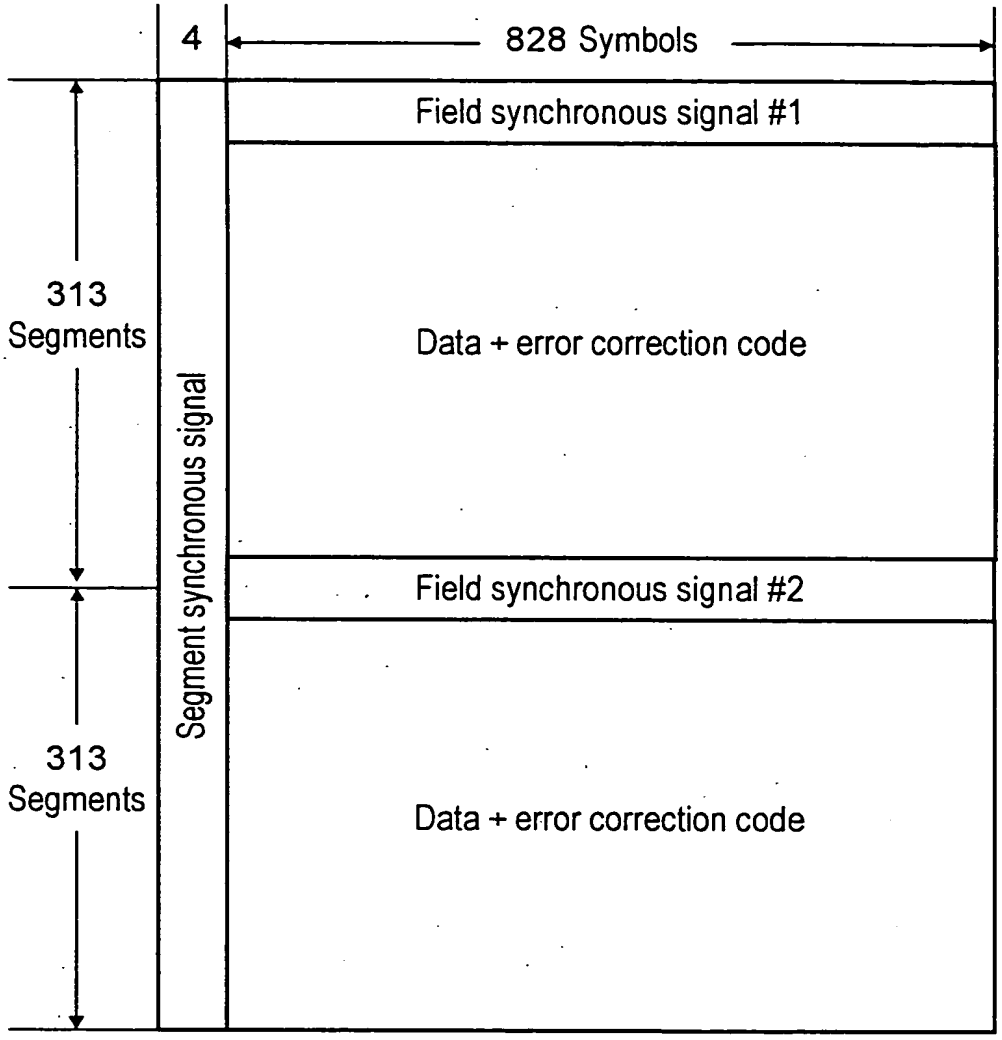

4
828 Symbols
Field synchronous signal #1
313
Segments
Data + error correction code
Segment synchronous signal
Field synchronous signal #2
313
Segments
Data + error correction code

FIG. 6

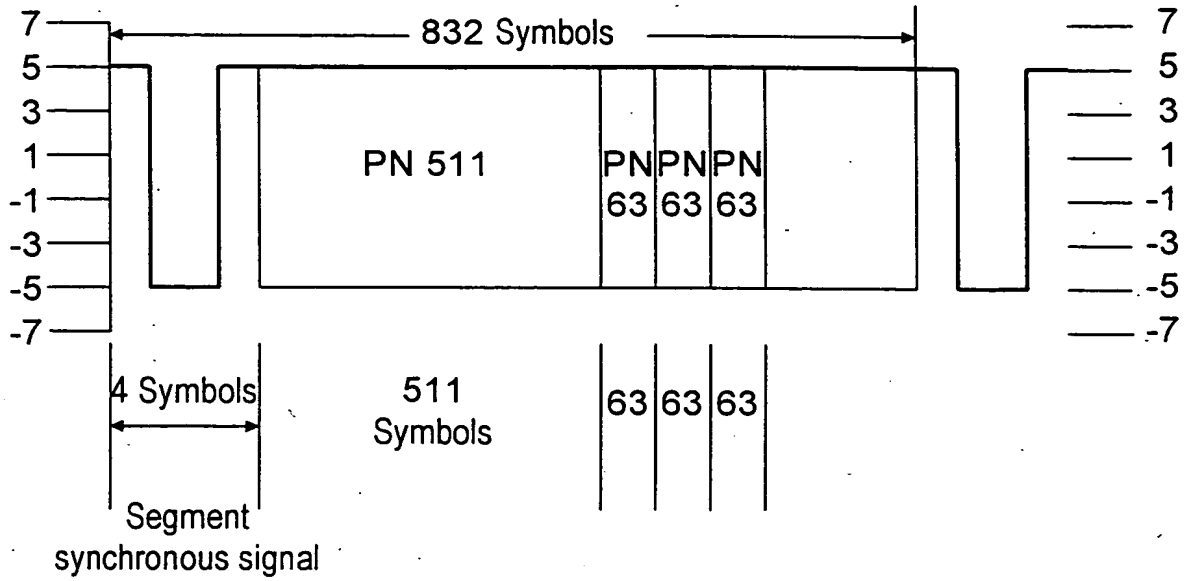

7
5
3
1
-1
-3
-5
-7
832 Symbols
PN 511
PN 63
PN 63
PN 63
4 Symbols
511 Symbols
63
63
63
Segment synchronous signal

FIG. 7

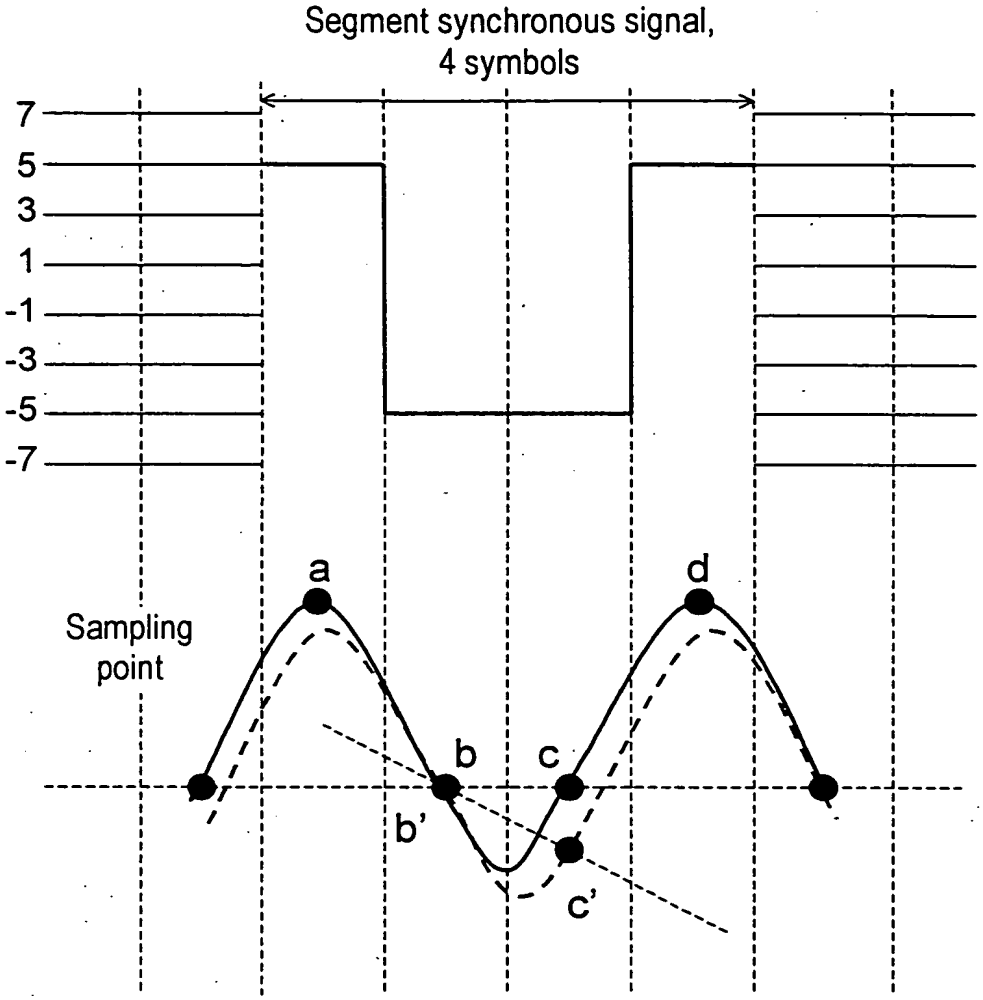

Segment synchronous signal,
4 symbols
7
5
3
1
-1
-3
-5
-7
Sampling
point
a
b
c
d
b'
c'

FIG. 8

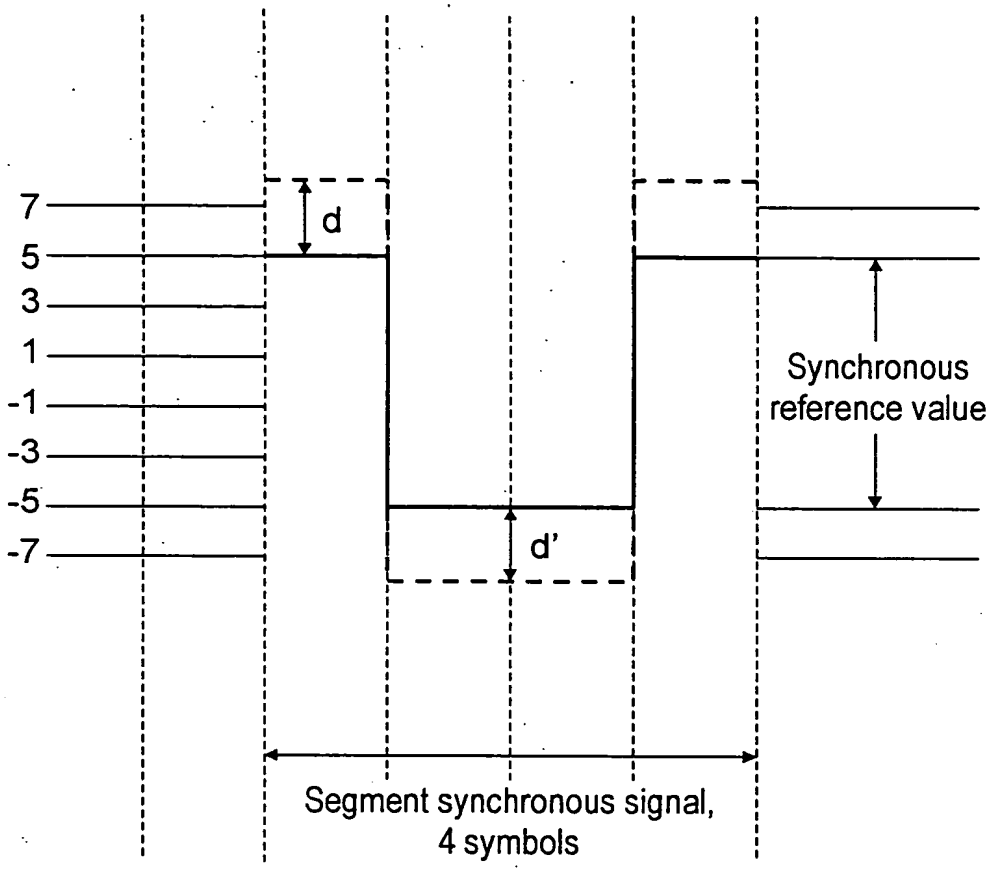

7
5
3
1
-1
-3
-5
-7
d
d'
Synchronous reference value
Segment synchronous signal, 4 symbols

FIG. 9

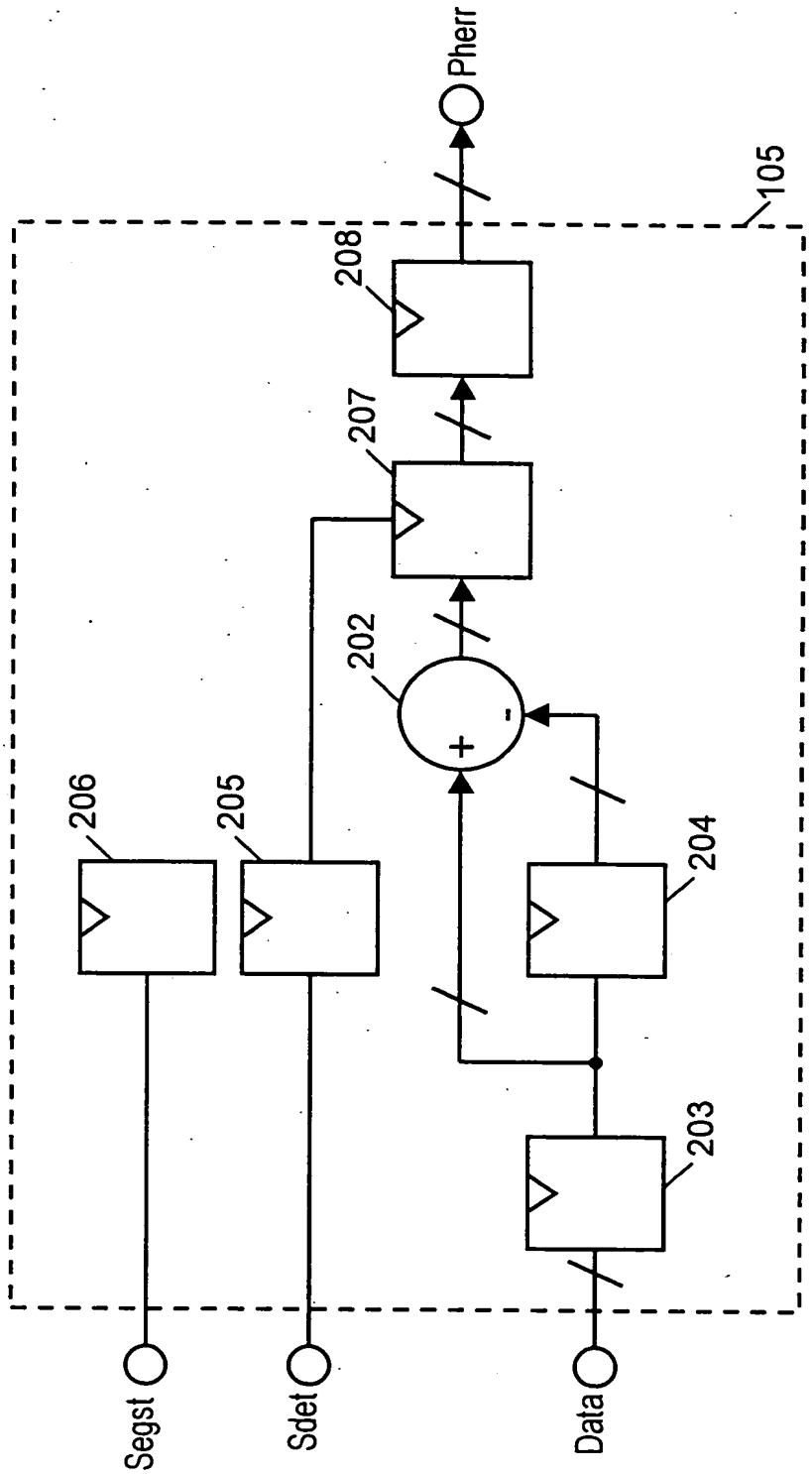
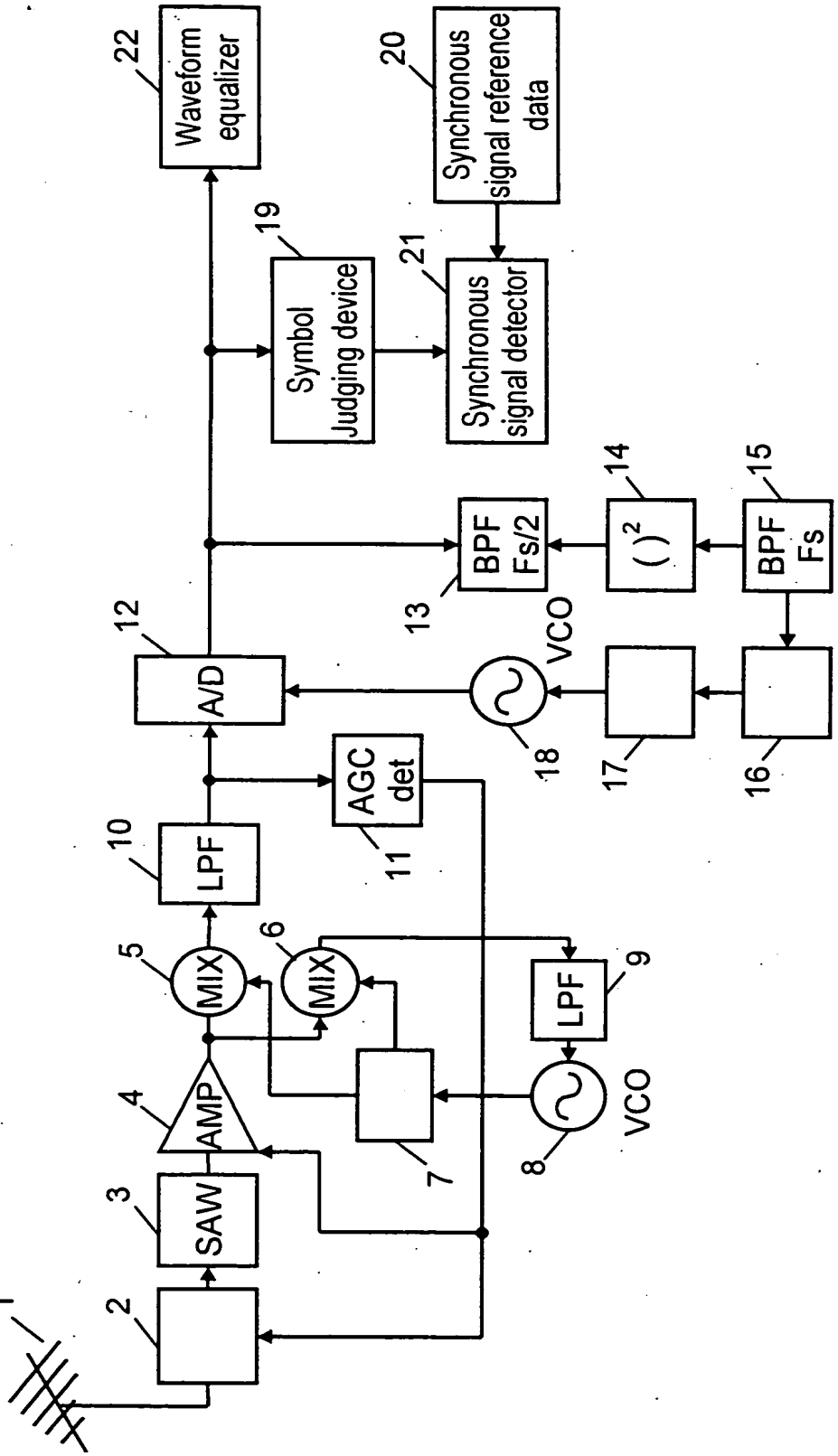


FIG. 10


1
2
3
SAW
4
AMP
5
MIX
6
MIX
7
8
VCO
9
LPF
10
LPF
11
AGC det
12
A/D
13
BPF Fs/2
14
( )²
15
BPF Fs
16
17
18
VCO
19
Symbol Judging device
20
Synchronous signal reference data
21
Synchronous signal detector
22
Waveform equalizer

Reference Numerals

1	Reception antenna
2	Digital broadcast tuner
3	SAW filter
4	Analog amplifier for amplifying signal
5, 6	Mixer
7	90-degree phase shifter
8, 18	Voltage control oscillator (VCO)
9, 10	Low pass filter (LPF)
11	AGC detector for detecting signal envelope
12	A/D converter
13	Band pass filter for passing frequency component of 1/2 of symbol speed
14	Square circuit
15	Band pass filter for passing frequency component of symbol speed Fs
16	Phase detector for detecting phase error
17	Loop filter
19	Symbol judging device
20	Synchronous signal reference data
21	Synchronous signal detector
22	Waveform equalizer
101	Synchronous code pattern detecting circuit
102	Symbol number counter
103	Detection protection counter
104	Segment synchronism detection establishing circuit
105	Clock phase error detecting circuit
106	AGC error detecting circuit
107	AGC control signal terminal
108	Clock regeneration control signal terminal

109 Segment start signal (Segst) terminal

110 Segment synchronism establishing (Shld) terminal

112, 114 D/A converter

113, 115 LPF

116 Segment synchronism detection establishing block

202 Subtractor

203, 204, 205, 206, 207, 208 Latch

Co Count-up signal

Data Digital data

Gerr Error signal

Lo Output signal

MSB Most significant bit

Pherr Clock regeneration control signal

Sdet Code pattern detection signal

Segst Segment start signal

Shld Segment synchronism establishing signal

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 99/05339

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04H1/00 H04N7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 375 693 A (KUHN WILLIAM B) 1 March 1983 (1983-03-01) column 1, line 1 -column 3, line 40; claim 1	1,4,7,8, 10
A	WO 96 02990 A (LOENROTH BRIAN ;RINGSET VIDAR (NO); HD DIVINE (SE); ROTH GOERAN (S) 1 February 1996 (1996-02-01) page 1, line 1 -page 12, line 16; claim 1; figure 1	1,4,7,8, 10
A	US 5 477 199 A (MONTREUIL LEO) 19 December 1995 (1995-12-19) column 1, line 1 -column 4, line 15; claim 1	1,4,7,8, 10

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 December 1999	21/01/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	De Haan, A.J.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 136 292 A (ISHIDA HISAKI) 4 August 1992 (1992-08-04) column 1, line 1 -column 4, line 2; claim 1; figure 1	1,4,7,8, 10
A	DE 25 41 187 A (PHILIPS NV) 25 March 1976 (1976-03-25) page 1, line 1 -page 4, line 22; claims 1-3; figure 1	1,4,7,8, 10
A	WO 94 11968 A (AMPEX SYSTEMS CORP) 26 May 1994 (1994-05-26) page 1, line 1 -page 4, line 13; claim 1; figure 1	1,4,7,8, 10
A	US 5 673 293 A (SCARPA CARL G ET AL) 30 September 1997 (1997-09-30) column 1, line 1 -column 2, line 25; claim 1; figure 1	1,4,7,8, 10
A	EP 0 769 873 A (PARADYNE CORP) 23 April 1997 (1997-04-23) column 1, line 1 -column 3, line 44; claim 1; figure 1	1,4,7,8, 10
A	EP 0 769 364 A (SAMSUNG ELECTRONICS CO LTD) 23 April 1997 (1997-04-23) page 2, line 1 - line 43; claim 1; figure 1	1,4,7,8, 10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 99/05339

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US 4375693 A	01-03-1983	NONE		
WO 9602990 A	01-02-1996	AU	2994495 A	16-02-1996
		CN	1152982 A	25-06-1997
		JP	10505471 T	26-05-1998
		SE	9402464 A	14-01-1996
US 5477199 A	19-12-1995	US	5596606 A	21-01-1997
		AU	3683595 A	02-05-1996
		BR	9509229 A	27-01-1998
		CN	1160461 A	24-09-1997
		GB	2309141 A	16-07-1997
		WO	9611526 A	18-04-1996
		AU	684364 B	11-12-1997
		AU	2241295 A	23-10-1995
		AU	3761297 A	18-12-1997
		CA	2186853 A	12-10-1995
		CN	1147318 A	09-04-1997
		EP	0754368 A	22-01-1997
		JP	9511631 T	18-11-1997
		WO	9527330 A	12-10-1995
		US	5592513 A	07-01-1997
US 5136292 A	04-08-1992	DE	69030858 D	10-07-1997
		DE	69030858 T	29-01-1998
		EP	0417314 A	20-03-1991
		WO	9010903 A	20-09-1990
		JP	2525082 B	14-08-1996
		KR	9702390 B	05-03-1997
DE 2541187 A	25-03-1976	NL	7412226 A	18-03-1976
		AU	500993 B	07-06-1979
		AU	8488075 A	24-03-1977
		BE	833468 A	16-03-1976
		BR	7505928 A	03-08-1976
		CA	1069588 A	08-01-1980
		CH	593588 A	15-12-1977
		DK	409075 A	17-03-1976
		FR	2285031 A	09-04-1976
		GB	1506517 A	05-04-1978
		IT	1042538 B	30-01-1980
		JP	1044866 C	30-04-1981
		JP	51055607 A	15-05-1976
		JP	55035027 B	11-09-1980
		SE	7510163 A	17-03-1976
		US	4074199 A	14-02-1978
WO 9411968 A	26-05-1994	EP	0669063 A	30-08-1995
		US	5349611 A	20-09-1994
		US	5392289 A	21-02-1995
US 5673293 A	30-09-1997	NONE		
EP 0769873 A	23-04-1997	US	5841814 A	24-11-1998
		CA	2187380 A	18-04-1997
		JP	9200285 A	31-07-1997
EP 0769364 A	23-04-1997	JP	9233438 A	05-09-1997

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 99/05339

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0769364 A		US 5796786 A	18-08-1998